REMARKS

This paper is responsive to non-final Office Action dated October 24, 2003. Claims 1-32 were examined. Claims 12 and 13 are objected to for including informalities. Claims 20-32 stand rejected under 35 U.S.C. § 112, first paragraph. Claims 11, 17, 19, 23, 24, and 31 stand rejected under 35 U.S.C. § 112, second paragraph. Claims 1-19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,591,383 to Michel et al. Claims 1-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,835,501 to Dalmia et al. Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalmia in view of U.S. Patent No. 5,764,651 to Bullock et al. Claims 16-19 stand rejected over Michel in view of Dalmia. Claims 20-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalmia. Claims 24-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalmia in view of U.S. Patent No. 5,305,323 to Lada. Claims 31 and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalmia in view of Bullock.

Proposed Changes to the Drawings

Figure 18 has been changed to couple register 1205 to node 512 and to couple delay path 1815 to clock signal 514, consistent with the specification. No new matter has been added.

Claim Objections

Claim 12 is objected to as being indefinite for failing to particularly point out and distinctly claim the subject matter. Claim 12 is believed to be in allowable form. That form is used in numerous patents issued by the USPTO, including patents issued for classes 714/733 and 714/735. See, for example, claim 16 of U.S. Patent No. 6,675,335 of class 714/733 to Chiang et al., reciting "[t]he method of claim 15, further comprising storing..." and claim 2 of U.S. Patent No. 6,681,360 of class 714/735 to Ayrignac, reciting "[t]he method according to claim 1 further comprising repeating the inhibiting and observing....".

Claim 13 has been amended to recite the word "comprising."

Claim Rejections under 35 U.S.C. § 112, first paragraph

Claims 20-32 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Regarding claim 20, the Office Action states that "[c]laim 20 claiming 'a method of making a tested integrated circuit' does not comprise any steps pointing out of 'making an integrated circuit.'" Applicant respectfully points out that "[t]he transitional term 'comprising', which is synonymous with 'including,' 'containing,' or 'characterized by,' is inclusive or open-ended and does not exclude additional unrecited elements or method steps." See MPEP § 2111.03 (emphasis added). 35 U.S.C. § 112, first paragraph, states that

> [t]he specification shall contain a written description of the invention and the manner and process of making and using it, in full, clear concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

See 35 U.S.C. § 112, first paragraph (1999) (emphasis added). In addition, "[t]he claimed invention as a whole may not be adequately described if the claims require an essential or critical feature which is not adequately described in the specification and which is not conventional in the art or known to one of ordinary skill in the art." See MPEP § 2163 I. A (emphasis added). Applicant respectfully maintains that claims 20-22 are supported by the specification at least beginning at page 30, line 19, and satisfies the requirements of 35 U.S.C. § 112, first paragraph. Accordingly, Applicant respectfully requests that the rejection of claims 20-22 be withdrawn.

Regarding claim 23, claim 23 recites limitations directed to a bit error detect circuit and a counter circuit included in the integrated circuit for receiving an input data stream. In addition, the claim includes the transitional term "comprising," "which is synonymous with 'including,' 'containing,' or 'characterized by,' is inclusive or open-ended and does not exclude additional unrecited elements or method steps." See MPEP § 2111.03. Applicant respectfully maintains that enablement of claims 23-30 is supported by the specification at least by FIG. 1, 2, 5, 12A, 12B, 18, 19, 23, and 41 and related portions of the specification and satisfies the requirements of 35 U.S.C. § 112, first paragraph. Accordingly, Applicant respectfully requests that the rejection of claims 23-30 be withdrawn.

Regarding claim 31, claim 31 recites a phase zone detect circuit, a counter circuit, and a compare circuit included in an integrated circuit for determining an out-of-lock condition with respect to an input data stream. In addition, claim 31 includes the transitional term "comprising," "which is synonymous with 'including,' 'containing,' or 'characterized by,' is inclusive or open-ended and does not exclude additional unrecited elements or method steps." See MPEP § 2111.03. Applicant respectfully maintains that enablement of claims 31 and 32 is supported by the specification at least by FIG. 1, 2, 5, 12A, 12B, 18, 19, 23, and 41 and related portions of the specification and satisfies the requirements of 35 U.S.C. § 112, first paragraph. Accordingly, Applicant respectfully requests that the rejection of claims 31 and 32 be withdrawn.

Claim Rejections under 35 U.S.C. § 112, second paragraph

Claims 11, 17, 19, 23, 24, and 31 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Regarding claim 11, the Office Action rejects the language "...determining if a phase-locked loop..." and suggests the alternate language "...determining the locking of..."

> In reviewing a claim for compliance with 35 U.S.C. 112, second paragraph, the examiner must consider the claim as a whole to determine whether the claim apprises one of ordinary skill in the art of its scope and, therefore, serves the notice function required by 35 U.S.C. 112, second paragraph >by providing clear warning to others as to what constitutes infringement of the patent<....if the language used by applicant satisfies the statutory requirement of 35 U.S.C. 112, second paragraph, but the examiner merely wants the applicant to improve the clarity or precision of the language used, the claim must not be rejected under 35 U.S.C. 112, second paragraph, rather, the examiner should suggest improved language to the applicant.

See MPEP § 2173.02. Applicant submits that the original language of claim 11 is such that a person of ordinary skill in the art could interpret the metes and bounds of the claim so as to avoid infringement, and a rejection under 35 U.S.C. § 112, second paragraph is inappropriate. Accordingly, Applicant respectfully requests that the rejection of claim 11 withdrawn.

Claim 17 has been amended to recite "determining a bit error rate" to clarify the "determining." Accordingly, Applicant respectfully requests that the rejection of claim 17 withdrawn.

Regarding claim 23, the Office Action rejects the claim under 35 U.S.C. § 112, second paragraph based on the language "a bit error detect circuit coupled to determine if a bit error occurs..." and states that the circuit "should be coupled to something." Applicant respectfully disagrees.

> Functional language does not, in and of itself, render a claim improper. *In re Swinehhart*, 439 F.2d 210, 169, USPQ 226 (CCPA 1971). A functional limitation must be evaluated and considered, just like any other limitation of the claim, for what it fairly conveys to a person of ordinary skill in the pertinent art in the context in which it is used.

See MPEP § 2173.05(g). The limitations of claim 23 define the particular capability or purpose that is served by each of the bit error detect circuit and the counter circuit. These limitations define structural attributes of interrelated components of the claimed integrated circuit and comply with 35 U.S.C. § 112, second paragraph. Accordingly, Applicant respectfully requests that the rejection of claim 23 be withdrawn.

Regarding claim 24, the Office Action rejects the claim under 35 U.S.C. § 112, second paragraph based on the language "a first data path and a second data path coupled to receive the input data stream..." and states that the circuit "should be coupled to something." Applicant respectfully disagrees. See MPEP § 2173.05(g). The limitations of claim 24 define the particular capability or purpose that is served by the first and second data path. These limitations define structural attributes of interrelated components of the claimed integrated circuit and comply with 35 U.S.C. § 112, second paragraph. Accordingly, Applicant respectfully requests that the rejection of claim 24 be withdrawn.

Regarding claim 31, the Office Action rejects the claim under 35 U.S.C. § 112, second paragraph based on the language "a phase zone detect circuit coupled to determine..." and states that the circuit "should be coupled to something." Applicant respectfully disagrees. See MPEP § 2173.05(g). The limitations of claim 31 define the particular capability or purpose that is served by the phase zone detect circuit. This limitation define structural attributes of interrelated

components of the claimed integrated circuit and complies with 35 U.S.C. § 112, second paragraph. Accordingly, Applicant respectfully requests that the rejection of claim 31 be withdrawn.

Art Rejections under 35 U.S.C. § 102

Claims 1-19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,591,383 to Michel et al. Regarding claim 1, Applicant respectfully maintains that Michel, alone or in combination with other references of record, fails to teach or suggest

> determining over a plurality of first time intervals whether at least one transition of the input data stream occurred in a predetermined phase zone of a sample clock used to sample the input data stream,

as recited in claim 1. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)." See MPEP § 2131 (emphasis added). Michel teaches detecting an error rate of a data stream by counting the number of bad blocks in a detection interval to a threshold value. Abstract. Michel also teaches at col. 5, lines 20-35, computing errors with a BIP2 calculation, "comprising a 2-bit result in which one bit is the XOR of all of the even bits in a given data frame, and the other bit is the XOR of all of the odd bits." Nowhere does Michel teach or suggest a phase zone of a sample clock used to sample the input data stream or determining over a plurality of first time intervals whether at least one transition of the input data stream occurred in a predetermined phase zone of the sample clock. For at least this reason, Applicant respectfully maintains that claim 1 distinguishes over Michel and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 1, and all claims dependent thereon, be withdrawn.

Regarding claim 11, Applicant respectfully maintains that Michel, alone or in combination with other references of record, fails to teach or suggest

> determining over a plurality of first time intervals whether at least one transition of the input data stream occurred in a predetermined phase zone of a sample clock used to sample the input data stream

as recited in claim 11. Michel teaches detecting an error rate of a data stream by counting the number of bad blocks in a detection interval to a threshold value. Abstract. Michel also teaches at col. 5, lines 20-35, computing errors with a BIP2 calculation, "comprising a 2-bit result in which one bit is the XOR of all of the even bits in a given data frame, and the other bit is the XOR of all of the odd bits." Nowhere does Michel teach or suggest a phase zone of a sample clock used to sample the input data stream or determining over a plurality of first time intervals whether at least one transition of the input data stream occurred in a predetermined phase zone of the sample clock. For at least these reasons, Applicant respectfully maintains that claim 11 distinguishes over Michel and all references of record. Accordingly, Applicant respectfully requests that the rejection of claim 11, and all claims dependent thereon, be withdrawn.

Regarding claim 13, Applicant respectfully maintains that Michel, alone or in combination with other references of record, fails to teach or suggest

> means for detecting transitions of the input data stream occurring in a predefined phase zone of a sample clock sampling the input data stream,

as recited in claim 13. Michel teaches detecting an error rate of a data stream by counting the number of bad blocks in a detection interval to a threshold value. Abstract. Michel also teaches at col. 5, lines 20-35, computing errors with a BIP2 calculation, "comprising a 2-bit result in which one bit is the XOR of all of the even bits in a given data frame, and the other bit is the XOR of all of the odd bits." Nowhere does Michel teach or suggest a phase zone of a sample clock sampling the input data stream or means for detecting transitions of the input data stream occurring in a predefined phase zone of the sample clock. For at least these reasons, Applicant respectfully maintains that claim 13 distinguishes over Michel and all references of record.

Accordingly, Applicant respectfully requests that the rejection of claim 13, and all claims dependent thereon, be withdrawn.

Regarding claim 15, Applicant respectfully maintains that Michel, alone or in combination with other references of record, fails to teach or suggest

> determining whether transitions of the input data stream fall into a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream,

as recited in claim 15. Michel teaches detecting an error rate of a data stream by counting the number of bad blocks in a detection interval to a threshold value. Abstract. Michel also teaches at col. 5, lines 20-35, computing errors with a BIP2 calculation, "comprising a 2-bit result in which one bit is the XOR of all of the even bits in a given data frame, and the other bit is the XOR of all of the odd bits." Nowhere does Michel teach or suggest a sample clock period of a sample clock utilized to sample the input data stream or determining whether transitions of the input data stream fall into a predetermined portion of a sample clock period of the sample clock. For at least these reasons, Applicant respectfully maintains that claim 15 distinguishes over Michel and all references of record. Accordingly, Applicant respectfully requests that the rejection of claim 15, and all claims dependent thereon, be withdrawn.

Art Rejections under 35 U.S.C. § 103

Claims 1-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,835,501 to Dalmia et al. Applicant respectfully maintains the Office Action fails to establish a *prima facie* case of obviousness.

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of the ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all claim limitations.

See MPEP § 2143. Dalmia, alone or in combination with other references of record, fails to teach or suggest

> determining over a plurality of first time intervals whether at least one transition of the input data stream occurred in a predetermined phase zone of a sample clock used to sample the input data stream

as recited in claim 1. Dalmia teaches varying the frequency or phase of a clock signal at a predetermined rate and determining the number of bit errors arising in a clock and data recovery unit. Dalmia teaches at col. 3, lines 32-40 a bit error test including "generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER tester 3 the number of bit errors that arise in the CRUs recovered data stream." Dalmia fails to teach or suggest a phase zone of a sample clock or determining over a plurality of first time intervals whether at least one transition of the input data stream occurred in a predetermined phase zone of the sample clock. The Office Action states that "one of ordinary skill in the art would use well known principles of the predetermined phase zone (divided zone) in order to provide definition of the bit error rate." Applicant respectfully requests that the Examiner provide references in support of this position and explain how these references can be properly combined with other references of record to teach Applicant's claimed determination of whether transitions of the input data stream in a predetermined phase zone of a sample clock revealed in claim 1. Applicant respectfully maintains that claim 1 distinguishes over Dalmia and all references of record. Accordingly, Applicant respectfully requests that the rejection of claim 1, and all claims dependent thereon, be withdrawn.

Regarding claim 11, Applicant respectfully maintains the Office Action fails to establish a *prima facie* case of obviousness. See MPEP § 2143. Dalmia, alone or in combination with other references of record, fails to teach or suggest

> determining over a plurality of first time intervals whether at least one transition of the input data stream occurred in a predetermined phase zone of a sample clock used to sample the input data stream

as recited in claim 11. Dalmia teaches varying the frequency or phase of a clock signal at a predetermined rate and determining the number of bit errors arising in a clock and data recovery

unit. Dalmia teaches at col. 3, lines 32-40 a bit error test including "generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER tester 3 the number of bit errors that arise in the CRUs recovered data stream." Dalmia fails to teach or suggest a phase zone of a sample clock or determining over a plurality of first time intervals whether at least one transition of the input data stream occurred in a predetermined phase zone of the sample clock. The Office Action states that "one of ordinary skill in the art would use well known principles of the predetermined phase zone (divided zone) in order to provide definition of the bit error rate." Applicant respectfully requests that the Examiner provide references in support of this position and explain how these references can be properly combined with other references of record to teach Applicant's claimed determination of whether transitions of the input data stream in a predetermined phase zone of a sample clock revealed in claim 11. Applicant respectfully maintains that claim 11 distinguishes over Dalmia and all references of record. Accordingly, Applicant respectfully requests that the rejection of claim 11, and all claims dependent thereon, be withdrawn.

Regarding claim 13, Applicant respectfully maintains the Office Action fails to establish a *prima facie* case of obviousness. See MPEP § 2143. Dalmia, alone or in combination with other references of record, fails to teach or suggest

> means for detecting transitions of the input data stream occurring in a predefined phase zone of a sample clock sampling the input data stream,

as recited in claim 13. Dalmia teaches varying the frequency or phase of a clock signal at a predetermined rate and determining the number of bit errors arising in a clock and data recovery unit. Dalmia teaches at col. 3, lines 32-40 a bit error test including "generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER tester 3 the number of bit errors that arise in the CRUs recovered data stream." Dalmia fails to teach or suggest a phase zone of a sample clock or detecting transitions of the input data stream occurred in a predefined phase zone of the sample clock. The Office Action states that "one of ordinary skill in the art would use well known principles of the predetermined phase zone (divided zone) in order to provide definition of the bit

error rate." Applicant respectfully requests that the Examiner provide references in support of this position and explain how these references can be properly combined with other references of record to teach Applicant's claimed detection of transitions of the input data stream in a predefined phase zone of a sample clock revealed in claim 13. Applicant respectfully maintains that claim 13 distinguishes over Dalmia and all references of record. Accordingly, Applicant respectfully requests that the rejection of claim 13, and all claims dependent thereon, be withdrawn.

Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalmia in view of U.S. Patent No. 5,764,651 to Bullock et al. Applicant respectfully maintains that the Office Action fails to establish a *prima facie* case of obviousness. Dalmia, alone or in combination with Bullock and/or other references of record, fails to teach or suggest

> determining whether transitions of the input data stream fall into a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream,

as recited in claim 15. The Office Action states that "Dalmia et al. does not explicitly point out to the 'sample clock.'" Thus Dalmia fails to teach or suggest determining whether transitions of the input data stream fall into a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream. Bullock fails to compensate for the shortcomings of Dalmia. Bullock teaches a variable length window for sampling of erred bits in a data stream. Abstract. Bullock fails to teach or suggest a predetermined portion of a sample clock period of a sample clock. The Office Action states that "one of ordinary skill in the art would use well known principles of the predetermined phase zone (divided zone) in order to provide definition of the bit error rate." Applicant respectfully requests that the Examiner provide references in support of this position and explain how these references can be properly combined with other references of record to teach Applicant's claimed determination of whether transitions of the input data stream in a predetermined phase zone of a sample clock revealed in claim 15. Applicant respectfully maintains that claim 15 distinguishes over Dalmia and Bullock, alone or

in combination with other references of record. Accordingly, Applicant respectfully requests that the rejection of claim 15, and all claims dependent thereon, be withdrawn.

Claims 20-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalmia. Regarding claim 20, Applicant respectfully maintains that the Office Action fails to establish a *prima facie* case of obviousness. The Office Action fails to point out where Dalmia teaches and Applicant maintains that Dalmia, alone or in combination with other references of record, fails to teach or suggest

> determining whether transitions of the input data stream fall into a predetermined portion of a sample clock period of a sample clock utilized to sample the input data stream.

Dalmia teaches varying the frequency or phase of a clock signal at a predetermined rate and determining the number of bit errors arising in a clock and data recovery unit. Dalmia teaches at col. 3, lines 32-40 a bit error test including "generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER tester 3 the number of bit errors that arise in the CRUs recovered data stream." Dalmia fails to teach or suggest a predetermined portion of a sample clock utilized to sample the input data stream or determining whether transitions of the input data stream fall into a predetermined portion of the sample clock. The Office Action states that "one of ordinary skill in the art would use well known principles of the predetermined phase zone (divided zone) in order to provide definition of the bit error rate." Applicant respectfully requests that the Examiner provide references in support of this position and explain how these references can be properly combined with other references of record to teach Applicant's claimed determination of whether transitions of the input data stream fall into a predefined phase zone of a sample clock revealed in claim 20.

In addition, Dalmia fails to teach or suggest

> monitoring the indication to determine satisfactory performance of the integrated circuit,

as recited in claim 20. The Office Action states that "Dalmia et al. does not limit the monitoring the indication, inherently suggesting the possibility to use any monitoring including monitoring the indication to determine satisfactory." While a teaching may be express or inherent, inherency is a stringent standard.

> To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 U.S.P.Q.2D (BNA) 1746, 1749 (Fed. Cir. 1991). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." Id. at 1269, 20 U.S.P.Q.2D (BNA) at 1749 (quoting *In re Oelrich*, 666 F.2d 578, 581, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981).

See *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999); MPEP § 2112. Applicants disagree that it is inherent for the system of Dalmia to practice the claim. For example, there is no teaching or suggestion that Dalmia must (or does) monitor the indication of a plurality of evaluation intervals having one or more transitions in the predetermined portion of the sample clock period to determine satisfactory performance of the integrated circuit. To be inherent in monitoring the indication of a plurality of evaluation intervals having one or more transitions in the predetermined portion of the sample clock period to determine satisfactory performance of the integrated circuit, those functions must by necessity be performed in Dalmia. They are not.

For at least these reasons, Applicant respectfully maintains that claim 20 distinguishes over Dalmia, alone or in combination with other references of record. Accordingly, Applicant respectfully requests that the rejection of claim 20, and all claims dependent thereon, be withdrawn.

Regarding claim 23, Applicant respectfully maintains that the Office Action fails to establish a *prima facie* case of obviousness. Applicant maintains that Dalmia, alone or in combination with other references of record, fails to teach or suggest

> a bit error detect circuit coupled to determine if a bit error occurs in the input data stream according to whether an input data stream transition occurs in a

predetermined phase zone of a sample clock used in the bit error detect circuit

as recited by claim 23. Dalmia teaches varying the frequency or phase of a clock signal at a predetermined rate and determining the number of bit errors arising in a clock and data recovery unit. Dalmia teaches at col. 3, lines 32-40 a bit error test including "generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER tester 3 the number of bit errors that arise in the CRUs recovered data stream." Dalmia fails to teach or suggest a phase zone of a sample clock or determining over a plurality of first time intervals whether at least one transition of the input data stream occurred in a predetermined phase zone of the sample clock. The Office Action states that "one of ordinary skill in the art would use well known principles of the predetermined phase zone (divided zone) in order to provide definition of the bit error rate." Applicant respectfully requests that the Examiner provide references in support of this position and explain how these references can be properly combined with other references of record to teach Applicant's claimed determination of whether transitions of the input data stream in a predetermined phase zone of a sample clock revealed in claim 23. Applicant respectfully maintains that claim 23 distinguishes over Dalmia, alone or in combination with other references of record. Accordingly, Applicant respectfully requests that the rejection of claim 23, and all claims dependent thereon, be withdrawn.

Claims 31 and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dalmia in view of Bullock. Applicant respectfully maintains that the Office Action fails to establish a *prima facie* case of obviousness. Dalmia, alone or in combination with Bullock and/or other references of record, fails to teach or suggest

a phase zone detect circuit coupled to determine if a transition of the input data stream occurs in a predetermined phase zone of a sample clock used to sample the input data stream,

as recited in claim 31. The Office Action admits that "Dalmia et al. does not explicitly point out to the 'sample clock'". Bullock teaches comparing bit interleave parity of a frame compared

with a calculated value for the frame. (Col. 6, lines 59-64) However, Bullock alone or in combination with other references of record, fails to teach a phase zone detect circuit coupled to determine if a transition of the input data stream occurs in a predetermined phase zone of a sample clock used to sample the input data stream. For at least this reason, Applicant respectfully maintains that claim 31 distinguishes over Dalmia, alone or in combination with other references of record. Accordingly, Applicant respectfully requests that the rejection of claim 31, and all claims dependent thereon, be withdrawn.

In summary, claims 1-32 are in the case. Claims 13 and 17 have been amended. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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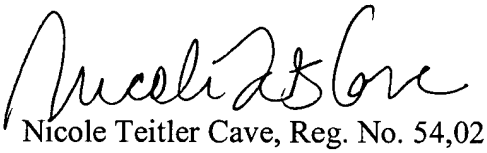

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